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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,868	12/10/2003	Han-Gu Sohn	8729-226 (ID-200306-011-1	6860

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/732,868	SOHN ET AL.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10 and 12-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-10 and 12-27* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities: The Examiner believes the semicolon after "comprises" on the third line should be a colon, instead. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-7, 10, 12-16, 20-21, and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Smolansky, et al., US Patent 5,673,396.

4. With respect to claim 1, Smolansky teaches a semiconductor memory device comprising:

an integrated circuit (IC) memory chip comprising an integrated memory circuit and a plurality of address pins, in col. 2, line 67 through col. 3, line 2, wherein the integrated memory circuit comprises:

a memory cell array, col. 3, lines 59-61, any of the memory spaces.

a data buffer for processing data read from or written to the memory cell array, in col. 2, lines 34-35.

a data width control circuit for selectively controlling a data width of the data buffer in response to one or more address bits of an external address signal, in col. 6, line 38, through col. 7, line 9, wherein the data width control circuit comprises:

a decoder for decoding the one or more address bits of external address signal in response to a data access command to generate a first control signal, in col. 6, lines 45-48; and

a data buffer controller, responsive to the first control signal, to generate a second control signal for controlling the data width of the data buffer, in col. 7, lines 23-45.

5. With respect to claim 3, Smolansky teaches the device of claim 1, wherein the data width control circuit selectively controls the data width of the data buffer by generating a control signal that masks or unmasks one or more bits of the data buffer, in col. 7, lines 23-45.

6. With respect to claim 4, Smolansky teaches the device of claim 3, wherein a masked bit is prevented from being input to the memory cell array from the data buffer, in col. 7, lines 23-45.

7. With respect to claim 5, Smolansky teaches the device of claim 3, wherein a masked bit is prevented from being output from the data buffer, in col. 7, lines 23-45.

8. With respect to claim 6, Smolansky teaches the device of claim 1, wherein the data buffer has a width of n bits and wherein the data width of the data buffer is selectively controlled to be n bits or less, in col. 2, lines 34-47.

9. With respect to claim 7, Smolansky et al. teach a decoder which comprises:

a switching circuit, in col. 4, lines 1-8; and

a logic circuit, wherein the switching circuit is response to the data access command to pass the external address signal to the logic circuit and wherein the logic circuit processes the external command to generate the first control signal based on the external command, in col. 10, line 65, through col. 11, line 10.

10. With respect to claims 10 and 12-16, these claims are similar to claims 1 and 3-7, except that they are claimed with an input and output data buffer instead of one data buffer. Smolansky teaches the use of an input and output data buffer in col. 5, lines 42-57. Therefore these claims are rejected using similar logic.

11. With respect to claim 20, Smolansky teaches an integrated circuit (IC) memory device, comprising:

a memory data buffer; and a data width control circuit for selectively varying a data width of the memory data buffer in response to an external control signal applied to one or more address pins of the IC memory device, in col. 6, line 38, through col. 7, line 9.

12. With respect to claim 21, Applicant claims a memory system comprising a controller for generating data access command signals and address signals, and the semiconductor memory device of claim 1, but does not contain the last two limitations of claim 1, and is therefore rejected using similar logic.

13. With respect to claim 25, Applicant claims a method for providing data I/O width control in a semiconductor memory device similar to claim 1, but excluding the last two limitations of claim 1, and is therefore rejected using similar logic.

14. With respect to claim 26, Applicant claims a semiconductor memory device similar to claim 1, but excluding the last two limitations of claim 1, and is therefore rejected using similar logic.

15. With respect to claim 27, Applicant claims a semiconductor memory device similar to claim 1, but excluding the last two limitations of claim 1, and is therefore rejected using similar logic.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. Claims 8-9, 17-19 rejected under 35 U.S.C. 103(a) as being unpatentable over Smolansky as applied to claims 1 and 16 above, in view of Miyata, US Patent 4,706,219.

19. With respect to claim 8, Miyata et al. teach the device of claim 7, wherein the logic circuit comprises a plurality of parallel connected AND gates that receive the external address signal, and wherein the first control signal comprises a plural bit signal comprised of the output signals from the AND gates, in col. 6, lines 15-19.

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Smolansky and Miyata before him at the time the invention was made, to modify the variable data length storage memory of Smolansky with the variable data length storage memory of Miyata et al., so that a variety of integrated circuit memories can be inexpensively produced at high productivity as a result of having a variable word length, as taught by Miyata in col. 1, lines 39-44.

21. With respect to claim 9, Miyata teaches the device of claim 8, wherein the data buffer controller comprises:

a switching circuit comprising a plurality of parallel connected switches, wherein each switch receives the data access command, and wherein one or more switches are selectively activated in response to the first control signal to generate the second control signal, the second control signal comprise a plural bit signal comprised of the output signals of the switches, in fig. 7.

22. With respect to claims 17-19, these are similar to claims 8-9, except applied to parent claim 10, which contains both an input and an output data buffer. Therefore claims 17-19 are rejected using similar reasoning as claims 8-9.

23. Claims 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smolansky claims 20 and 21 above, in view of Hirai, US Patent 5,349,448.

24. With respect to claim 22, Smolansky teaches all limitations of the parent claims, but fail to explicitly describe that the controller is a microprocessor unit. Hirai teaches that the controller for use in the present invention can be a microprocessor unit, in col. 1, lines 32-35.

25. It would be obvious to one of ordinary skill in the art having the teachings of Smolansky and Hirai before him at the time the invention was made, to modify the invention of Smolansky with the invention of Hirai to use a microprocessor unit as a controller in a storage system, because microprocessors are extremely well known in the art as ways to implement a controller.

26. With respect to claim 23, Smolansky teaches all limitations of the parent claims, but fail to explicitly describe that the controller is a network control unit. Hirai teaches that the controller for use in the present invention can be a network control unit, in col. 1, lines 40-41.

27. It would be obvious to one of ordinary skill in the art having the teachings of Smolansky and Hirai before him at the time the invention was made, to modify the invention of Smolansky with the invention of Hirai to use a microprocessor unit as a controller in a storage system, because microprocessors are extremely well known in the art as ways to implement a controller.

28. With respect to claim 24, Smolansky teaches all limitations of the parent claims, but fail to explicitly describe that the controller is a memory controller. Hirai teaches that

the controller for use in the present invention can be a memory controller, in col. 1, lines 32-35 and fig.1, where it is obvious that the controller controls image memory and is therefore a memory controller.

29. It would be obvious to one of ordinary skill in the art having the teachings of Smolansky and Hirai before him at the time the invention was made, to modify the invention of Smolansky with the invention of Hirai to use a microprocessor unit as a controller in a storage system, because microprocessors are extremely well known in the art as ways to implement a controller.

Response to Arguments

30. Applicant's arguments, see amendments and remarks, filed 7/6/07, with respect to the rejection(s) of claim(s) 1, 3-10, and 12-27 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Smolansky.

Conclusion

31. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

32. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory systems.

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Ryan Dare/
Ryan Dare
September 15, 2007

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